Response #11
M. Brunsman
10/1/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Morishita, Y.

Serial No.: 09/619,669 Group Art Unit: 2814

Filed: July 19, 2000 Examiner: Nguyen, D.

For: AN INPUT/OUTPUT PROTECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231

RESPONSE UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated July 17, 2002, please consider the following.

REMARKS

Claims 1-27, all of the claims pending in the present Application, stand rejected under 35 USC §103(a) as unpatentable over Applicant's Admitted Prior Art (Figures 5A and 5B), further in view of US Patent 5,945,713 to Voldman.

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed (e.g., in claim 1), the present invention is directed to an input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring. A first diffusion layer is fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite the first